What is claimed is:

1. A circuit comprising:

a plurality of entries, each of the entries having a number of cells including at least a first cell and a second cell;

an output port having a number of selecting units including at least a first selecting unit coupled to the first cell of each of the entries and a second selecting unit coupled to the second cell of each of the entries; and

a match port having a number of comparing units including at least a first comparing unit coupled to the first cell of each of the entries and a second comparing unit coupled to the second cell of each of the entries.

2. The circuit of claim 1, wherein the first selecting unit includes:

a first multiplexing portion to select a selected first cell, the selected first cell being the first cell of one of the entries; and

a second multiplexing portion coupled to the first multiplexing portion to transfer data from the selected first cell to a global bit line.

3. The circuit of claim 1, wherein the first comparing unit includes a number of comparators to compare data from the first cell of each of the entries with a reference data.

4. The circuit of claim 3, wherein each of the comparator includes a logic unit to perform a logic function on data from the first cell of each of the entries with the reference data.

5. The circuit of claim 1, wherein the number of the selecting units is equal to the number of comparing units.

6. An integrated circuit comprising:

a plurality of entry groups, each of the entry groups including multiple entries, each of the entries including multiple cells, the cells being grouped into a number of bit groups, each of the bit groups including one cell from each of the entries;

a plurality of output ports, each of the output ports including multiple selecting units; each of the selecting units including input nodes coupled to a corresponding bit group, the corresponding bit group being one of the bit groups; and

a plurality of match ports, each of the match ports including multiple comparing units; each of the comparing units including input nodes coupled to the corresponding bit group.

7. The integrated circuit of claim 6, wherein each of the selecting units includes:

a number of local bit lines;

a number of selectors, each of the selectors including a plurality of first switches coupled to one of the local bit lines, each of the first switches coupling to one cell of the corresponding bit group; and

a number of second switches, each of the second switches coupling between one of the local bit lines and a precharge node.

8. The integrated circuit of claim 7, wherein each of the comparing units includes a plurality of comparators, each of the comparators coupling to one cell of the corresponding bit group and to a reference node.

9. The integrated circuit of claim 8, wherein each of the comparators includes a pair of pass gates coupled to one cell of the corresponding bit group and to the reference node.

10. The integrated circuit of claim 7, wherein each of the selecting units further includes a precharger to charge the precharge node to an initial value.

11. The integrated circuit of claim 10, wherein each of the first switches includes a pair of transistors coupled in series between one of the local bit lines and a supply node.

12. The integrated circuit of claim 11, wherein a number of first switches equals a number of entries in each of the entry groups.

13. The integrated circuit of claim 6 further comprising an input controller having a plurality of word lines, each of the word lines coupling to one of the entries.

14. The integrated circuit of claim 13 further comprising a plurality of decoders, each of the decoders coupling to one of the output ports.

15. A system comprising:

an integrated circuit including,

a register array to store data, the register array including at least one entry group having multiple entries, each of the entries including multiple cells, the cells being grouped into a number of bit groups, each of the bit groups including one cell from each of the entries;

at least one output port to output the data from the register array, the at least one output port having a number of selecting units; each of the selecting units coupling to one of the bit groups; and at least one match port to compare the data stored in the register array with reference data, the at least one match port having a number of comparing units, each of the comparing units coupling to one of the bit groups; and

a dynamic random access memory device coupled to the integrated circuit.

16. The system of claim 15, wherein each of the selecting units includes:

a first multiplexing portion to select a cell in one of the bit groups; and

a second multiplexing portion coupled to the first multiplexing portion to transfer data from the cell to a global bit line.

17. The system of claim 16, wherein each of the comparing units includes a number of comparators to compare data from one of the bit groups with a reference data.

18. The system of claim 17 further comprising a decoder coupled to the at least one output port.

19. The system of claim 15, wherein the number of the selecting units is equal to the number of bit groups.

20. The system of claim 15, wherein the number of the comparing units is equal to the number of bit groups.

21. The system of claim 15, wherein the integrated circuit includes a processor.

22. A method comprising:

accessing a group of entries, each of the entries having a number of bits including at least a first bit and a second bit, the first bit of each of the entries being grouped into a first bit group, the second bit of each of the entries being grouped into a second bit group;

comparing the first bit of each of the entries with a first reference bit;

comparing the second bit of each of the entries with a second reference bit; and

activating at least one match signal if the first bit of a selected one of the entries matches the first reference bit and if the second bit of the selected one of the entries matches the second reference bit.

23. The method of claim 22, wherein accessing includes simultaneously accessing the first bit of each of the entries.

24. The method of claim 22 further comprising:

reading bits in the first bit group to a first selector; and

reading bits in the second bit group to a second selector.

25. The method of claim 24 further comprising:

selectively transferring a bit from the first selector to a first global bit line; and

selectively transferring a bit from the second selector to a second global bit line.

26. The method of claim 22, wherein comparing the first bit of each of the entries with the first reference bit occurs simultaneously.

27. The method of claim 26, wherein comparing the second bit of each of the entries with the second reference bit occurs simultaneously with the comparing the first bit of each of the entries with the first reference bit.